WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Friday, February 04, 2005

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L6	L4 same process$4	13
☐	L5	L4 same parallel$9	0
☐	L4	L3 same synchroniz$9	41
☐	L3	l1 same L2	102
☐	L2	(generat$4 near2 (module or local) near2 clock)	1591
☐	L1	(generat$4 near2 (system or main or central) near2 clock)	6334

END OF SEARCH HISTORY

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Friday, February 04, 2005

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L6	l5 same process$5	5
☐	L5	(synchroniz$9 near5 (local adj clock) near5 ((system or main or central) adj clock))	20
☐	L4	L2 same (clock near5 fail$4)	14
☐	L3	L2 same (driv$4 near3 down near3 process$4)	0
☐	L2	L1 same synchroniz$9	318
☐	L1	((system or main) near2 clock) same (local$4 near2 clock)	902

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L6: Entry 4 of 5 File: USPT Apr 16, 1991

DOCUMENT-IDENTIFIER: US 5008805 A
TITLE: Real time, fail safe process control system and method

Detailed Description Text (3):
FIG. 2 is a more detailed functional block diagram of the sender processor 10 or the listener processor 20, both of which are identical in their hardware and software configurations. The processor 10, for example, includes a processor bus 33 to which is connected a central processing unit (CPU) 32, a magnetic storage DASD 34, a LAN1 adapter 36 which is connected to the LAN1, the LAN2 adapter 38 which is connected to the LAN2, and a programmable timer consisting of a co-processor 42 having an input connected to the local clock 40. The local clock 40 has a synchronizing clock input 23 connected to the system clock 22. The co-processor 42 manages the timer table 44 using the timer manager 61, which provides programmable timing which is essential to the operation of the processor 10. The memory 46 connected to the bus 33 stores a plurality of scheduling and execution tables as well as the various software modules necessary to execute the method of the invention.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L5: Entry 7 of 20 File: USPT Jul 3, 2001

DOCUMENT-IDENTIFIER: US 6256507 B1
** See image for Certificate of Correction **
TITLE: Telecommunications network synchronization for data services

CLAIMS:

20. The network as in claim 18 wherein the local clock within the mobile switching center is synchronized to a global positioning system clock pulse when the synchronization system is configured in the star network type topology mode of operation, and further including a local clock within each base station that is also synchronized to the global positioning system clock pulse when the synchronization system is configured in the star network type topology mode of operation.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L4: Entry 10 of 14 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870441 A
TITLE: Distributed clocking system

Brief Summary Text (18):
Another aspect of the invention provides for fast and automatic recovery in the event of any type of failure in the system master clock. According to this feature of the invention, when a switch element detects a failure in the transmission of the clock currently being used for synchronization, the switch element will immediately switchover to its own local clock for synchronization. Thereafter, the switch element detecting the failure will transmit the outgoing data synchronized to its own local clock along with its own clock rank and a notification of the detected failure on all of its outgoing communications links to the other switch elements in the system. In this manner, all of the switch elements in the system will eventually be notified of the failure and they will each begin selecting an alternate clock for synchronization. Eventually, the highest ranked clock in the system that is still functional will become the new system master clock for the entire network. If the failure mode was initiated as the result of a failure in a transmission link, rather than a failure in the master clock itself, the original master clock will retain the role of master clock for synchronizing the network operations.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L5: Entry 1 of 20 File: USPT Dec 28, 2004

DOCUMENT-IDENTIFIER: US 6836851 B2
TITLE: Two-step synchronization method in which two modules are synchronized first by frequency followed by a synchronization in phase

Brief Summary Text (4):
In the field of telecommunication and of computer technology, the assemblies of an appliance that are needed for operation can frequently not be disposed on one electronic printed circuit board, but have to be distributed over a plurality of separate modules each having one or more printed circuit boards. In the case of telecommunication systems, in particular, redundant modules are also used for fail-safe reasons. So that the modules operate synchronously, the modules are supplied with a central timing signal, also known as "clock signal". Such a central clock signal is generated by a central clock generator and transmitted to the modules. Provided for the transmission is, for example, a clock channel in a bus to which the modules are connected. The modules operate either directly with the clock signal picked up from the bus or synchronize a separate, local clock generator, present on the respective module, to the central clock signal. In the latter case the local clock generators each generate local clock signals that are slightly phase-shifted in relation to the central clock signal, which shift is due to the transit time of the central clock signal on the bus.

Previous Doc Next Doc Go to Doc#

L5: Entry 5 of 20 File: USPT Jul 8, 2003

DOCUMENT-IDENTIFIER: US 6591370 B1
TITLE: Multinode computer system with distributed clock synchronization system

Detailed Description Text (9):
In process block 68, base register 60 from local clock 19 is copied to base register 52 of local clock 18. During the read and write operation of process block 68, dynamic counters 50 and 62 have been incrementing and contain an elapsed time since synchronization line 56 was activated (i.e., depending on whether dynamic counter 50 is edge or level triggered, the dynamic counter 50 may store an elapsed time from the activation of the synchronization line 56 or an elapsed time since the synchronization line 56 is deactivated.) Once base register 52 is loaded with the clock value from base register 60, the local clock 18 is synchronized. In process block 70, the synchronized clock is obtained by adding the counts in dynamic counter 50 and base register 52 and providing their sum as the synchronized clock on output 58 of adder 54. Although the above-described example uses a predetermined local clock on node 13, any local clock in the system may be used. Alternatively, this system may include a central clock (not shown) similar to local clock 18 that is used to synchronize any local clocks on the nodes.

Detailed Description Text (10):
FIG. 6 shows another embodiment of a local clock 18 that may be used. In FIG. 6, local clock 18 includes a write register 82, an adder 84, and a clock register 86 (also called a dynamic register). Unlike the dynamic counters of FIG. 4, clock register 86 of FIG. 6 contains the total clock value of clock 18. Clock register 86 may be any desired size, such as 64 bits. In its normal mode of operation, clock register 86 increments once per cycle of the system clock 22 (however, a prescaler may be used). This incrementing of clock register 86 is effectuated by using a multiplexer 88, adder 84, and an AND gate 90. Multiplexer 88 is a 2:1 multiplexer having one input coupled to write register 82 and another input coupled to a constant (e.g., a logical 1). Multiplexer 88 outputs a 1 unless a write line 92 is activated. Adder 84 adds the logical 1 to the current value of clock register 86 and outputs to AND gate 90 this incremented value. During its normal mode of operation, the AND gate 90 passes this incremented value to clock register 86, which loads the value in synchronization with system clock 22. Thus, an output 94 of the clock 18 is the value of the local clock, which increments in synchronization with the system clock. If write line 92 is activated, multiplexer 88 passes the contents of write register 82 to adder 84 rather than a logical 1. Adder 84 then adds write register 82 to clock register 86 and the result is stored in clock register 86.

CLAIMS:

33. A multinode computer system having multiple nodes each with an associated local clock on the node, wherein at least two of the local clocks are to be synchronized with another one of the local clocks from one of the nodes, including a system clock wherein each node is coupled to the system clock without any intermediating nodes and includes at least one processor and a local clock having a dynamic register and a base register, a local clock operating in a first mode of operation wherein the dynamic register of the local clock is incremented in response to the system clock and a second mode of operation wherein a local clock is synchronized

L4: Entry 7 of 14 File: USPT Jan 23, 2001

DOCUMENT-IDENTIFIER: US 6178180 B1
TITLE: Communications adapter for processing ATM and ISDN data

Detailed Description Text (9):
The SC-bus switch 27 is the main clock source for all TDM clock functions, receiving a reference clock from one of the network interface driver and receiver modules 24, in a manner to be discussed with reference to FIG. 3. This clock signal is synchronized to an incoming data stream received from a network transmission line 7 or 7a. From this reference clock, the SC-bus switch 27 generates all main SC-bus clocks and all of the local port clocks. The local ports have a 4.096-Mhz bit clock and an 8-Khz frame synch clock, which are supplied to the network interface framer 25 and to the serial to parallel interface 21. When several communications adapter cards 10 are connected by the SC-bus 42, as shown in the example of FIG. 3, the SC-bus switch 27 of one of the cards 10 is programmed to be the master clock source, while the switches 27 on the other cards 10 are programmed to operate as slaves. In this way, the TDM data paths on all the cards 10 are synchronized to a single network cable 7. If this single clock source should fail, the SC-bus switches 27 have an ability to switch to another such switch 27 as an alternative master clock source, supporting a soft recovery mode of operation.

L4: Entry 3 of 14 File: USPT Jul 3, 2001

DOCUMENT-IDENTIFIER: US 6256507 B1
** See image for Certificate of Correction **
TITLE: Telecommunications network synchronization for data services

Detailed Description Text (8):
In response to an affirmative determination in either step 72 or step 74, the synchronization manager functionality reconfigures the synchronization system 12 in step 76 to operate in its second mode of operation wherein the local clock module is utilized as the primary reference source in a tree or linear network type topology (see, FIGS. 2B and 2C). In this mode, the local clock modules independently generate stratum 2 classified synchronization clock pulses to their associated mobile switching centers for use in deriving the system clock. Synchronization information is further conveyed to the base stations (who also derive the system clock) from each mobile switching center using the clock distribution system. While configured in the second mode of operation, the synchronization manager functionality of the transport network management system monitors network operation in step 78 for a failure of a local clock module. This second mode of operation (with a stratum 2 classified synchronization clock pulse supplied to the mobile switching centers and base stations) supports an absolute frequency tolerance with respect to synchronization of approximately +/-0.5 ppm. The synchronization manager functionality further monitors network operation in step 80 to detect any degradation in timing tolerances below an acceptable level (such as, for example, a degradation in measured absolute frequency tolerance exceeding +/-0.5 ppm). If neither determination of step 78 or step 80 is satisfied, the process for operation of the synchronization system remains in the second mode of operation (step 76) and continues to cycle through the determinations of step 78 and 80, unless a determination is made in step 82 that operation in the first mode is again available. If the determination of step 82 is affirmative (for example, if the global positioning system or GPS receiver becomes available, or if the measured absolute frequency tolerance satisfies the requisite threshold), the synchronization manager functionality reconfigures the synchronization system 12 in step 70 to operate in its first mode of operation.

L4: Entry 2 of 14 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6516422 B1
TITLE: Computer system including multiple clock sources and failover switching

Abstract Text (1):
A system and method for providing redundant, synchronized clocks in a computer system. Upon a failure of a master clock signal, the system switches over to a slave clock signal synchronized with the master clock signal. Switching logic is coupled to receive a first clock signal and a second clock signal. The switching logic selects either the first clock signal or the second clock signal as a local clock signal. The switching logic further monitors the first clock signal for a failure. If a failure is monitored, the switching logic accepts the second clock signal as the local clock signal in place of the first clock signal. One or more clock local loads operate according to the local clock signal. The switching logic may control the input to a phase locked loop (PLL) that provides the local clock signal to the local clock loads. The method includes a PLL synchronizing an output clock signal with the master clock signal. The output clock signal is used by at least one local clock load for timing. The switching logic monitors the master clock signal and the slave clock signal for a failure. Upon a failure of either the master clock signal or the slave clock signal, the switching logic notifies a system controller of the failure. Upon the failure of the first clock signal, the switching logic switches the second clock signal in place of the first clock signal as the master clock signal for the PLL, causes the second clock signal to fail-over and to take over as the master clock source to the PLL, and causes the second clock source to provide a reference control signal to the second clock source. Clock switching is automatic and does not interrupt or interfere with operation of the computer system.

Brief Summary Text (9):
The problems outlined above are in large part solved by a system and method for providing redundant, synchronized clocks in a computer system. Upon a failure of a master clock signal, the system switches over to a slave clock signal synchronized with the master clock signal. In one embodiment, switching logic is coupled to receive a first clock signal and a second clock signal. The switching logic is configured to select either the first clock signal or the second clock signal as a local clock signal. The switching logic is further configured to monitor the first clock signal for a failure. If a failure of the first clock signal is monitored, the switching logic is further configured to accept the second clock signal as the local clock signal in place of the first clock signal. The system also includes one or more clock local loads that operate according to the local clock signal. In another embodiment, the switching logic controls the input to a phase lock loop that provides the local clock signal to the local clock loads. This configuration may advantageously allow a redundant, synchronous slave clock to replace a master clock upon failure of the master clock.

Brief Summary Text (11):
A method is likewise contemplated for providing redundant, synchronous clock signals. The method comprises, in one embodiment, a first clock source providing a first clock signal as a master clock signal to a phase locked loop (PLL). A second clock source provides a second clock signal as a slave clock signal to the PLL, where the slave clock signal is synchronized with the master clock signal. The PLL

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L4: Entry 1 of 14 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665762 B2
TITLE: Computer having a plurality of plug-in cards

Brief Summary Text (12):
From DE 42 40 145 a system bus with a plurality of boards is known. If a master board fails, there will be no clock signal on the system bus and means are provided to generate clock signals locally on each board. The disadvantage of this system is, however, that the local clock signals are not synchronized to each other.

Previous Doc Next Doc Go to Doc#